

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

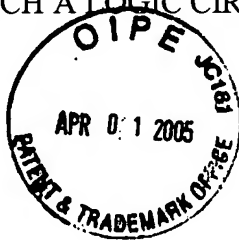
Applicant: Sunil Talwar et al.

Title: LOGIC CIRCUIT AND METHOD FOR CARRY AND SUM GENERATION AND METHOD OF DESIGNING SUCH A LOGIC CIRCUIT

Docket No.: 1365.063US1

Filed: November 14, 2003

Examiner: Unknown



Serial No.: 10/714,408

Due Date: N/A

Group Art Unit: 2124

MS Amendment

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

We are transmitting herewith the following attached items (as indicated with an "X"):

☒ A return postcard.

☒ A Supplemental Information Disclosure Statement (2 pgs.), Form 1449 (1 pg.). Two (2) non-U.S. documents enclosed. U.S. documents not enclosed pursuant to 37 C.F.R. 1.98(a)(2).

If not provided for in a separate paper filed herewith, Please consider this a **PETITION FOR EXTENSION OF TIME** for sufficient number of months to enter these papers and please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 30th day of March, 2005.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

Customer Number 21186

By: 

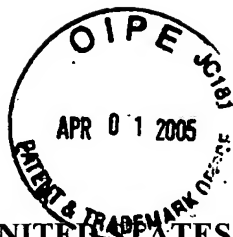
Atty: Timothy Clise

Reg. No. 40,957

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

(GENERAL)

S/N 10/714,408



PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Sunil Talwar et al.	Examiner:	Unknown
Serial No.:	10/714,408	Group Art Unit:	2124
Filed:	November 14, 2003	Docket:	1365.063US1
Title:	LOGIC CIRCUIT AND METHOD FOR CARRY AND SUM GENERATION AND METHOD OF DESIGNING SUCH A LOGIC CIRCUIT		

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Supplemental Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

Pursuant to 37 C.F.R. §1.97(b), it is believed that no fee or statement is required with the Supplemental Information Disclosure Statement. However, if an Office Action on the merits has been mailed, the Commissioner is hereby authorized to charge the required fees to Deposit Account No. 19-0743 in order to have this Supplemental Information Disclosure Statement considered.

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Serial No :10/714,408

Filing Date: November 14, 2003

Title: LOGIC CIRCUIT AND METHOD FOR CARRY AND SUM GENERATION AND METHOD OF DESIGNING SUCH A LOGIC CIRCUIT

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Pursuant to 37 C.F.R. 1.98(a)(2), Applicant believes that copies of cited U.S. Patents and Published Applications are no longer required to be provided to the Office. Notification of this change was provided in the United States Patent and Trademark Office OG Notices dated October 12, 2004. Thus, Applicant has not included copies of any US Patents or Published Applications cited with this submission. Should the Office require copies to be provided, Applicant respectfully requests that notice of such requirement be directed to Applicant's below-signed representative. Applicant acknowledges the requirement to submit copies of foreign patent documents and non-patent literature in accordance with 37 C.F.R. 1.98(a)(2).

The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

SUNIL TALWAR ET AL.

By their Representatives,

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(612) 349-9587

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 30th day of March, 2005.

Date

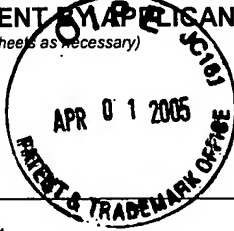
30 March '05

By

Timothy B Clise

Reg. No. 40,957

Substitute for form 1449A/PTO
**INFORMATION DISCLOSURE
 STATEMENT BY APPLICANT**
 (Use as many sheets as necessary)



Complete if Known

Application Number	10/714,408
Filing Date	November 14, 2003
First Named Inventor	Talwar, Sunil
Group Art Unit	2124
Examiner Name	Unknown

Sheet 1 of 1

Attorney Docket No: 1365.063US1

US PATENT DOCUMENTS

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Filing Date If Appropriate
	US-2004/0236814A1	11/25/2004	White, B. E.	01/12/2004
	US-3,843,876	10/22/1974	Fette, B. A., et al.	09/20/1973
	US-4,592,007	05/27/1986	Ohhashi, M.	09/29/1982
	US-4,713,790	12/15/1987	Kloker, K. L., et al.	07/31/1985
	US-4,866,658	09/12/1989	Mazin, M. , et al.	09/12/1988
	US-4,870,609	09/26/1989	Yasui, I. , et al.	10/26/1987
	US-5,343,418	08/30/1994	Zinger, R.	08/25/1992
	US-5,875,124	02/23/1999	Takahashi, H.	10/16/1997
	US-6,469,541	10/22/2002	Tran, D. J., et al.	12/05/2001
	US-6,700,405	03/02/2004	Hirairi, K.	12/01/2000

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	T ²
	JP-8212057 with English Abstract	08/20/1996	Takayanagi, N. , et al.	

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		HASHEMIAN, R. , "A Fast Carry Propagation Technique for Parallel Adders", <u>Proceedings of the 33rd Midwest Symposium on Circuits and Systems</u> , (1990),456-459	

EXAMINER

DATE CONSIDERED